

## Revision:3.1

www.xinxunwei.com 400-800-9990

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[illegible]

<b>GIGABYTE</b>			
Title			
<b>BLOCK DIAGRAM</b>			
Size	Document Number		Rev
Custom	<b>GA-M52LT-D3P</b>		<b>3.1</b>
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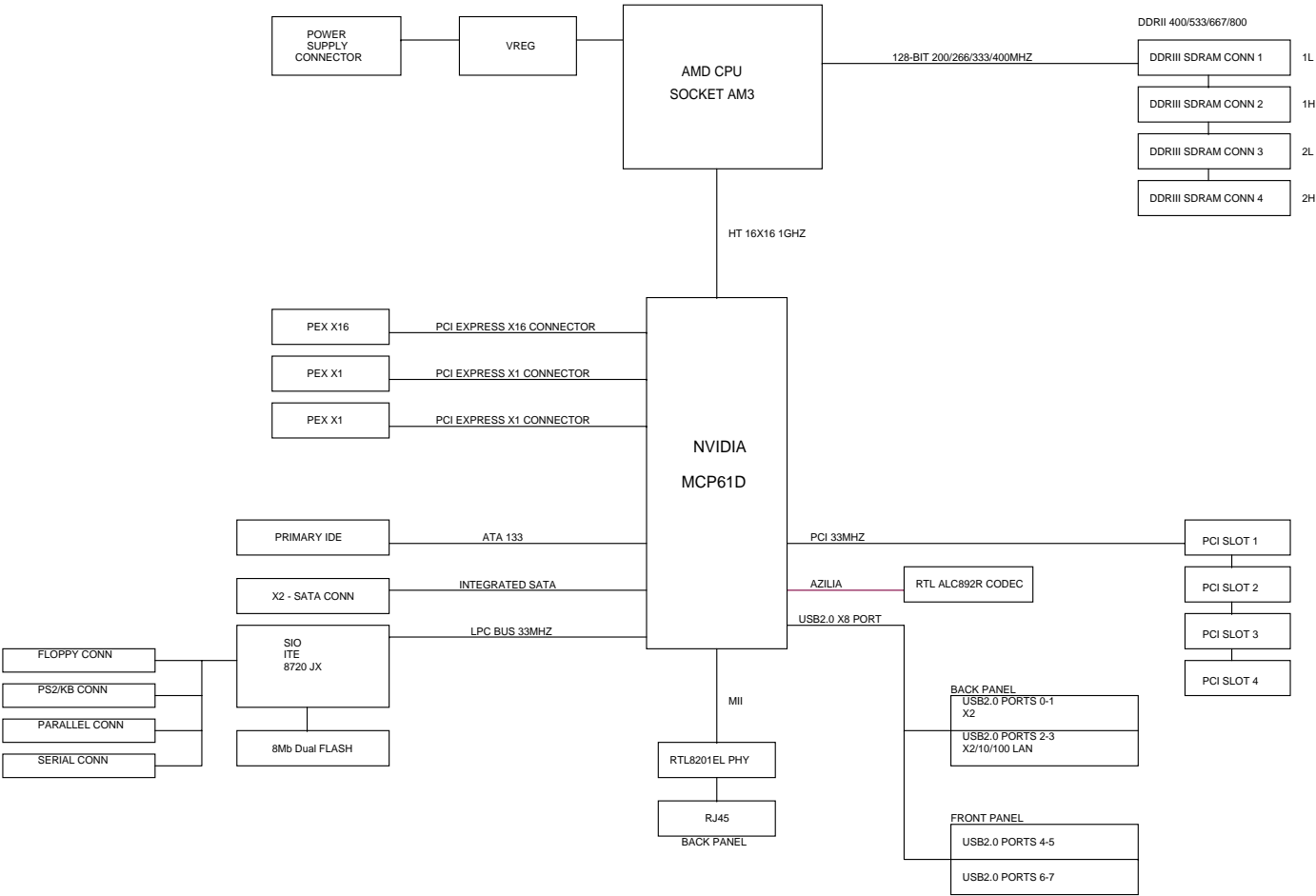
**P-Code: U96058-0**

[illegible]

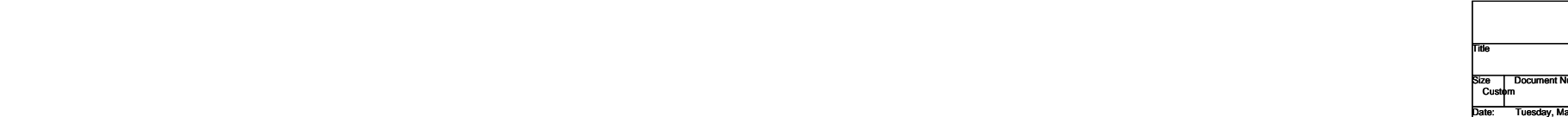
## Reason

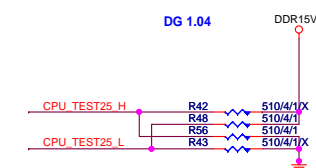
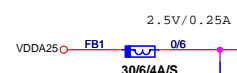
[illegible]

BLOCK DIAGRAM



```
CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT
```

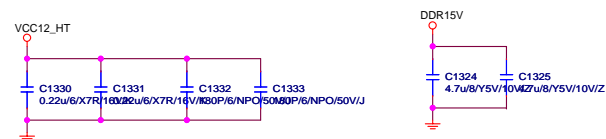
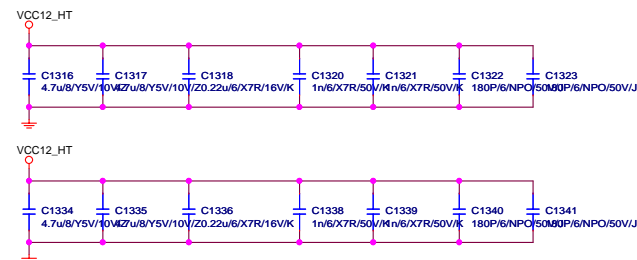
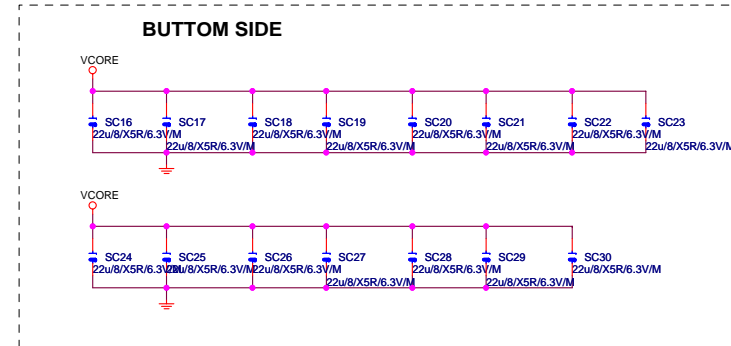
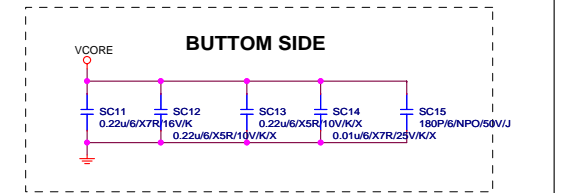
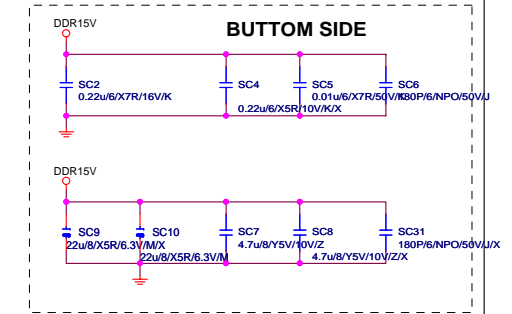
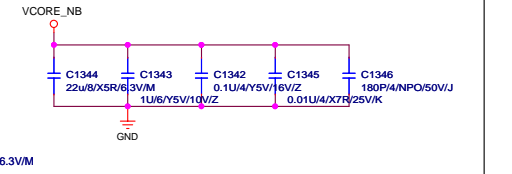




LAYOUT: Route trace 50 miles wide and 500 to 750 miles long between these caps.

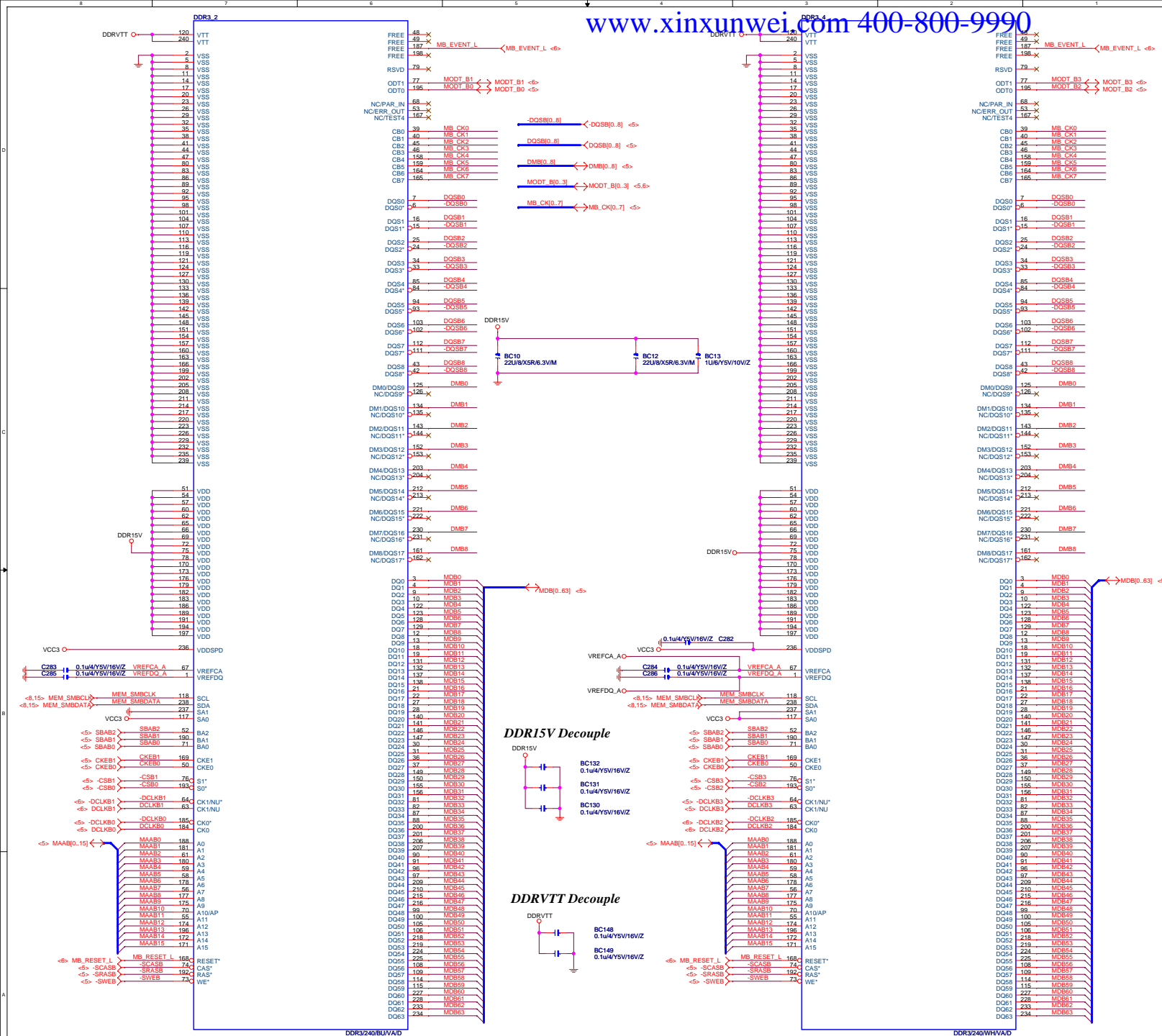


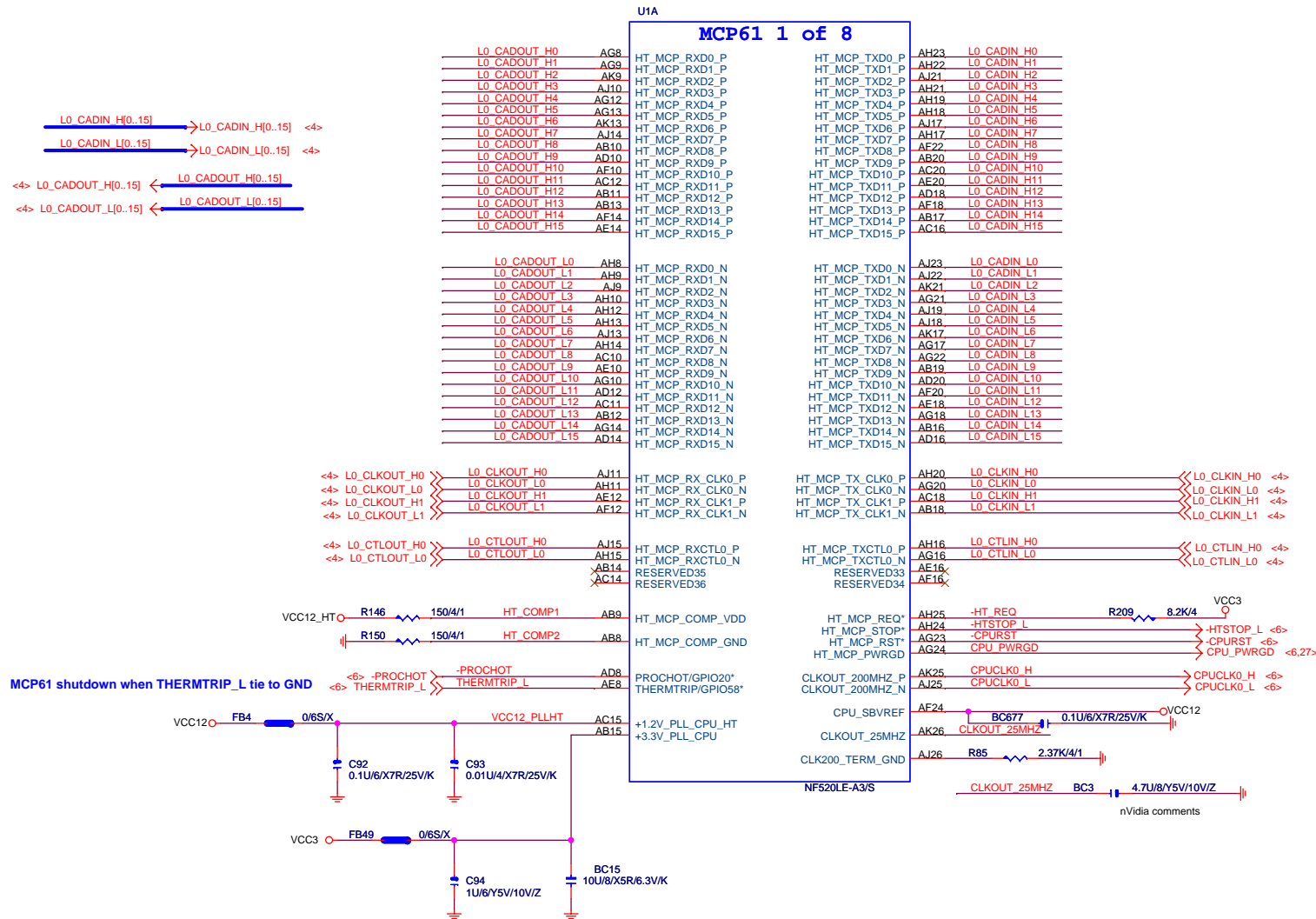
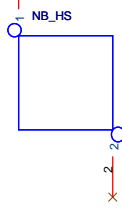
VLDT\_RUN\_B is connected to the VLDT\_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



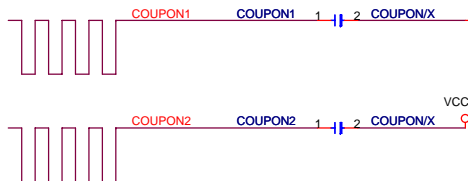




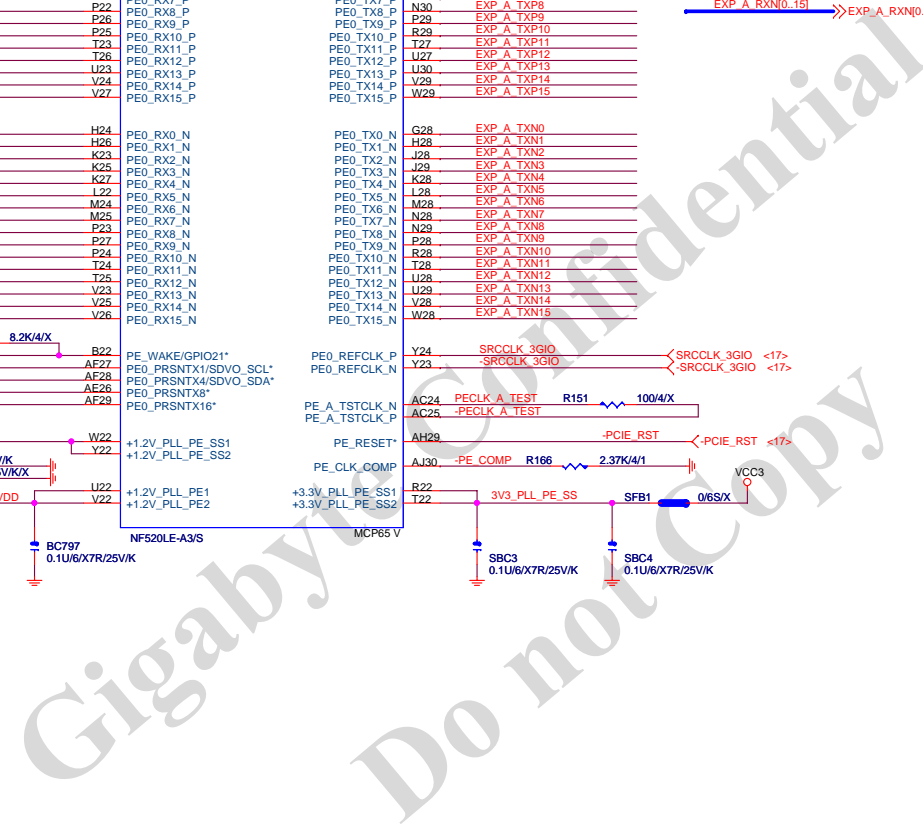


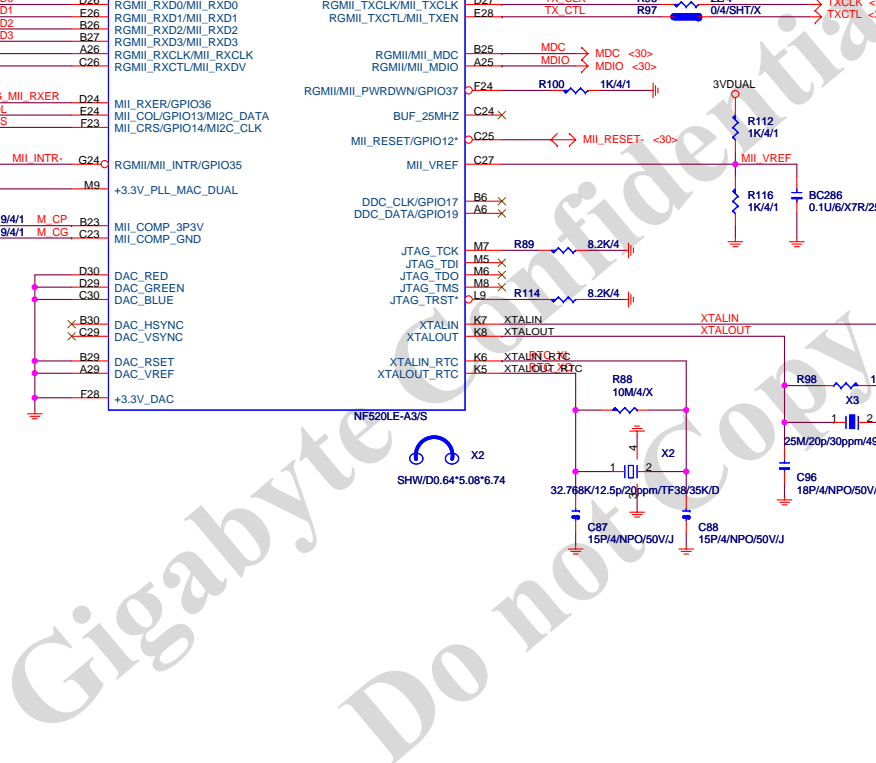
**N.B HEATSINK**

BGASINK\_NB[12SP2-01A004-02R]

**GIGABYTE**

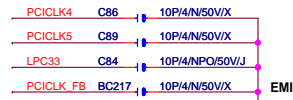
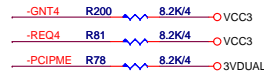
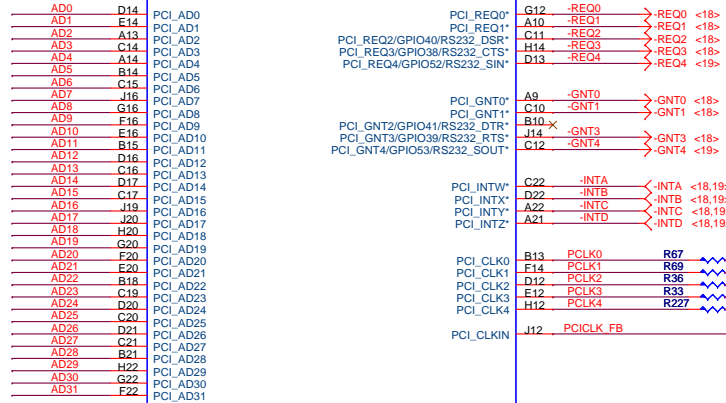
Title			
MCP61D-HOST			
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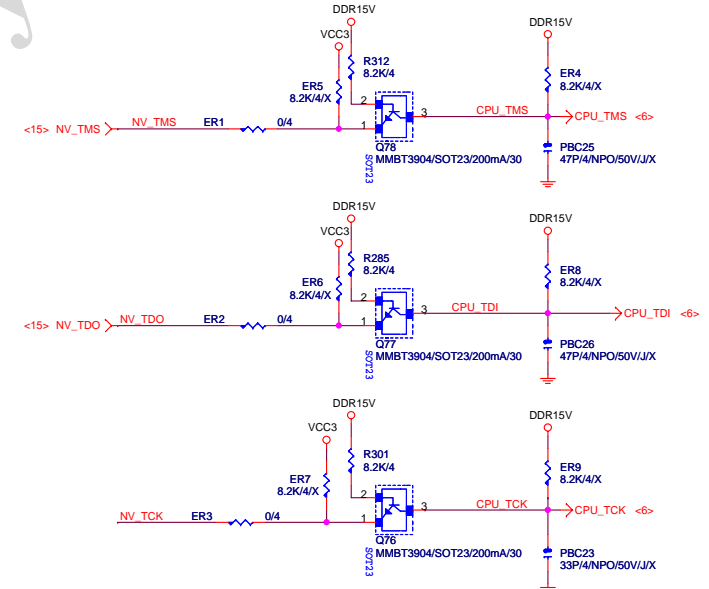


U1D

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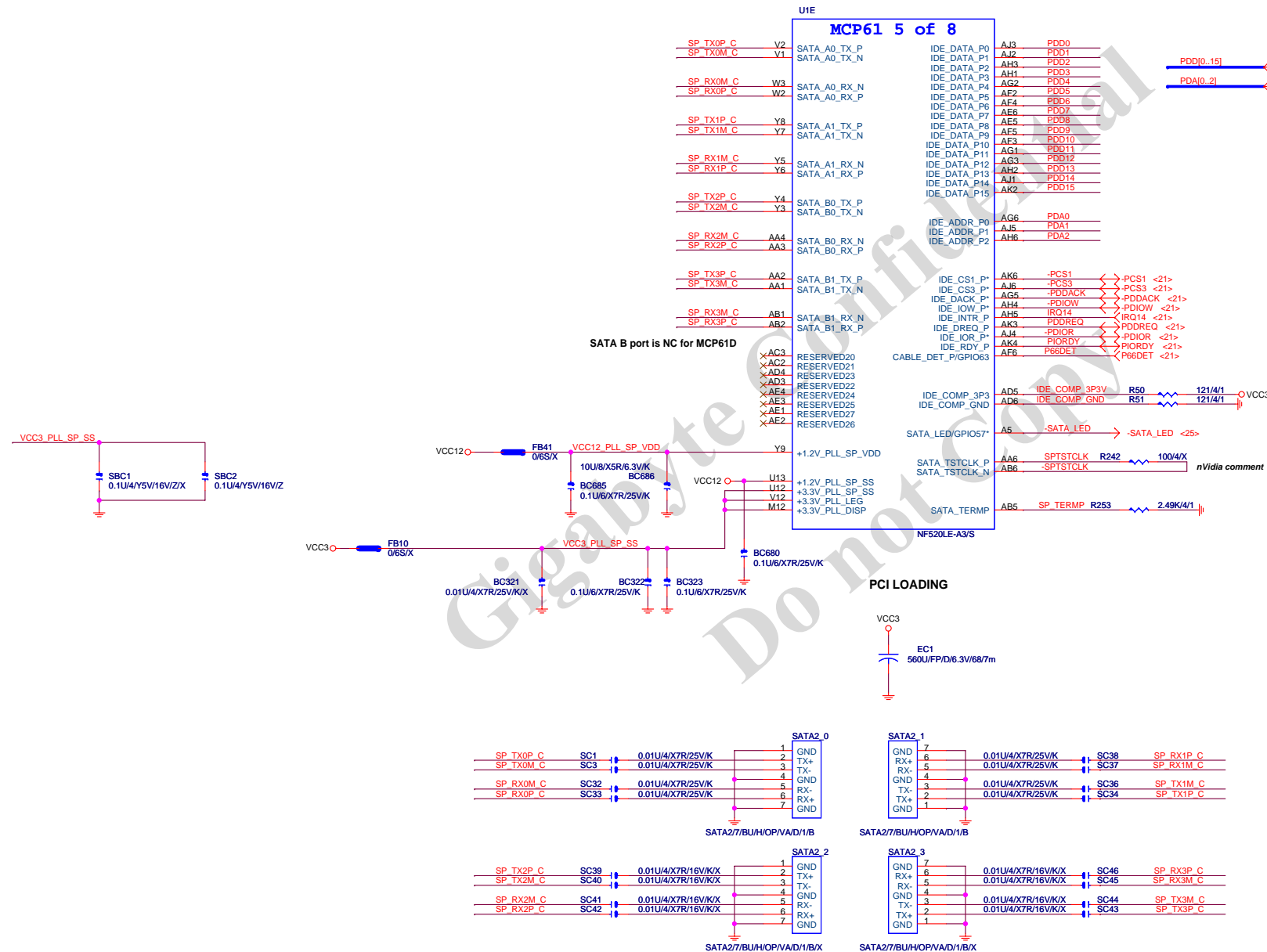


**BIOS STRAP:**  
 ACZ\_SDOUT  
 -LFRAME  
 00 = LPC BIOS  
 01 = PCI BIOS  
 10 = SPI BIOS(Default)  
 11 = RESERVED

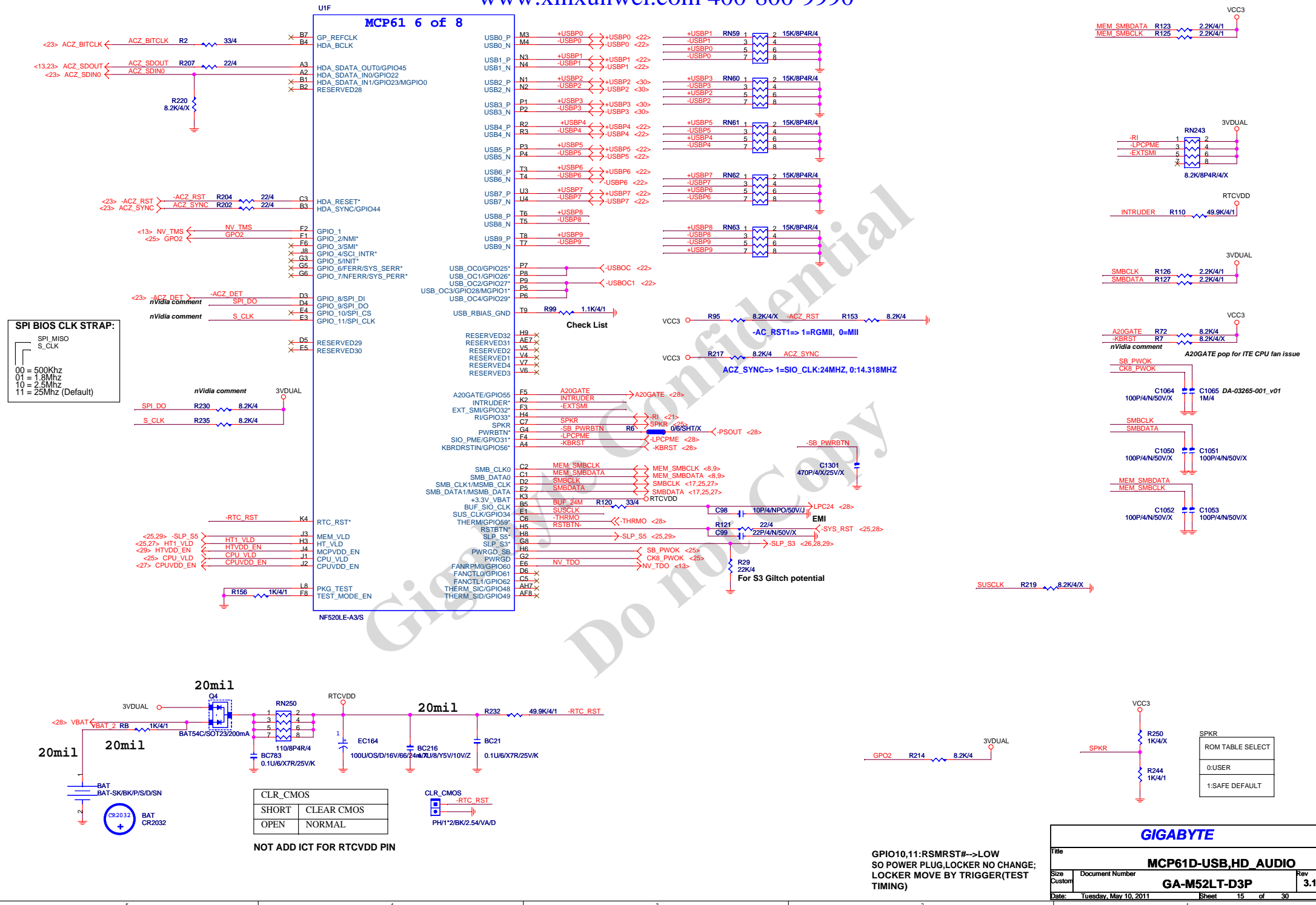


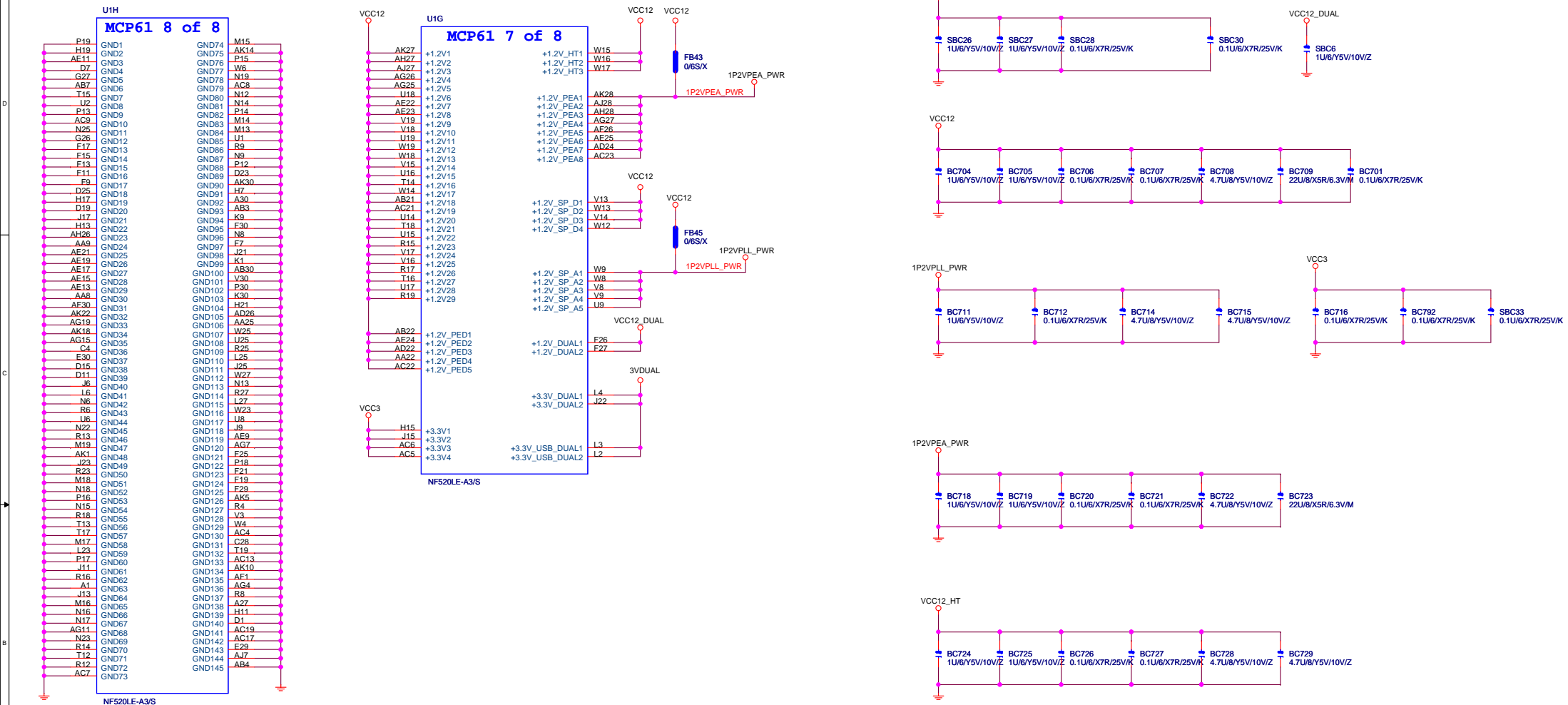
GIGABYTE

Title		
MCP61D-PCI BUS		
Size	Document Number	Rev
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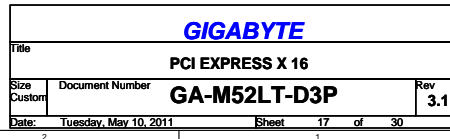
**GIGABYTE**Title  
**MCP61D-SATA IDE**

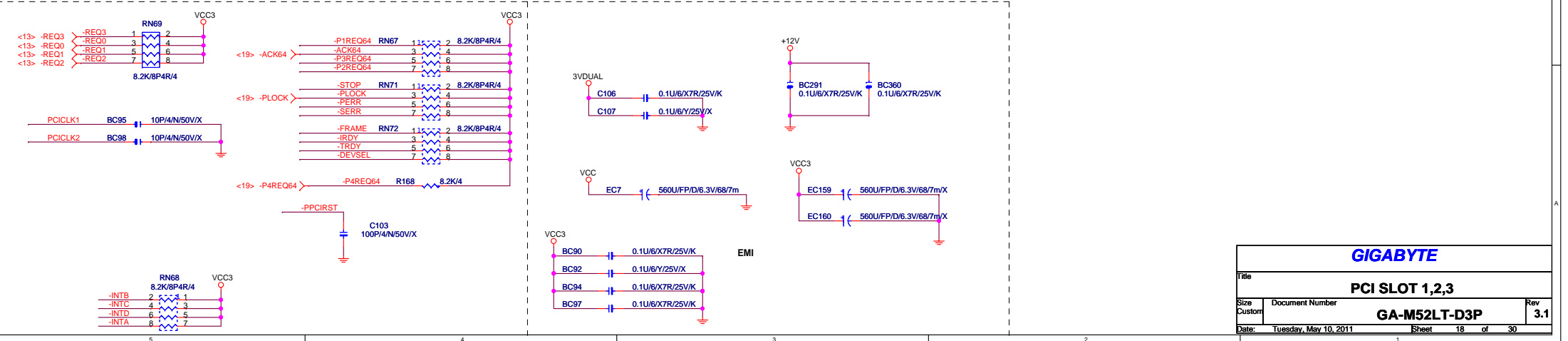
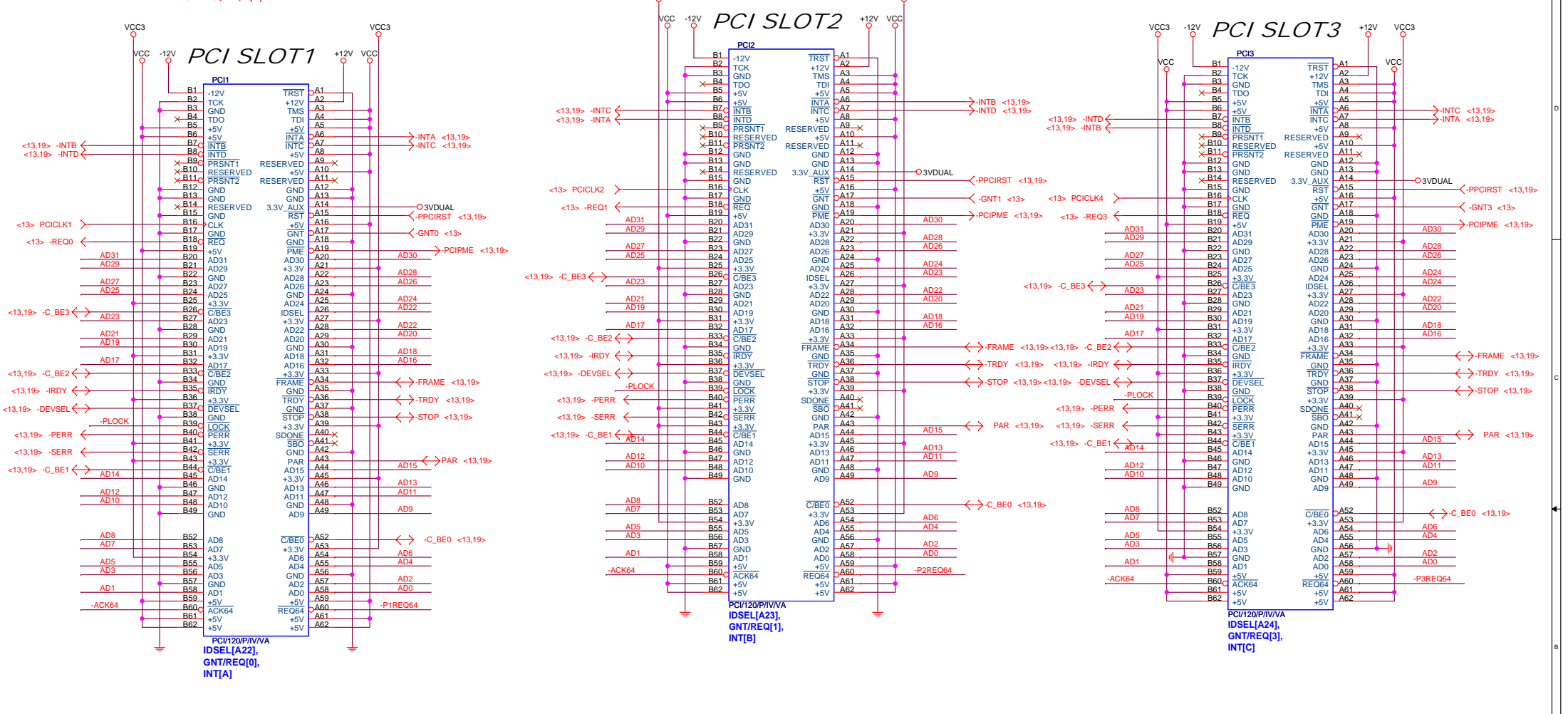
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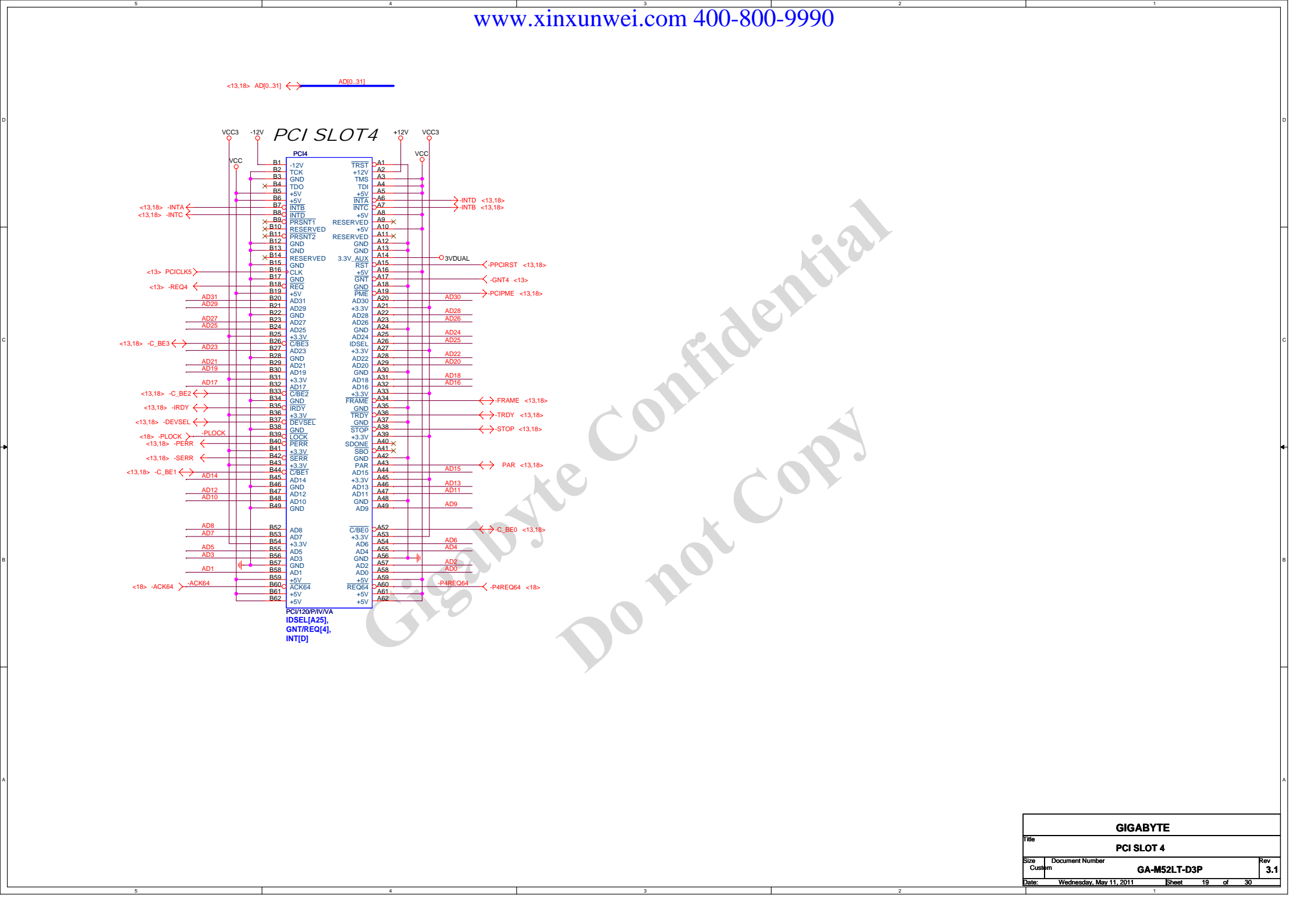




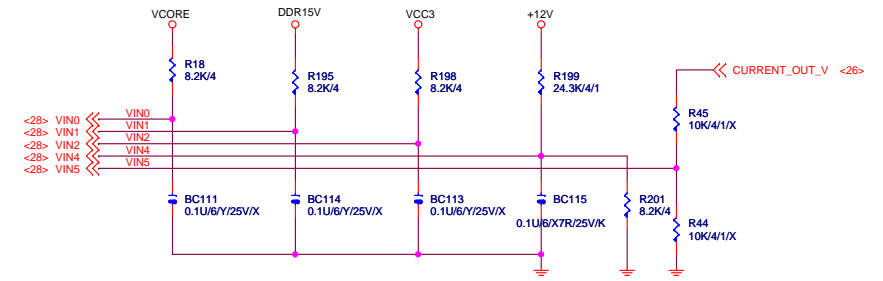
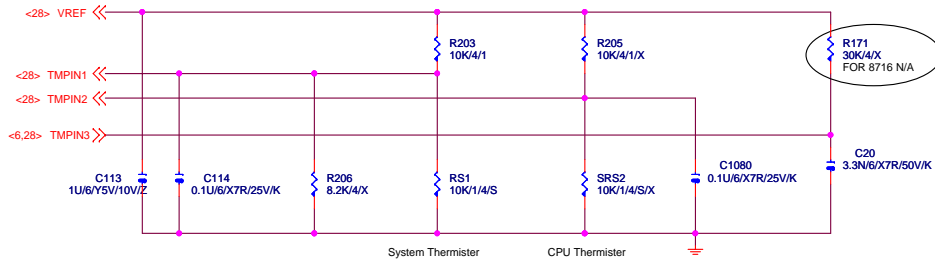




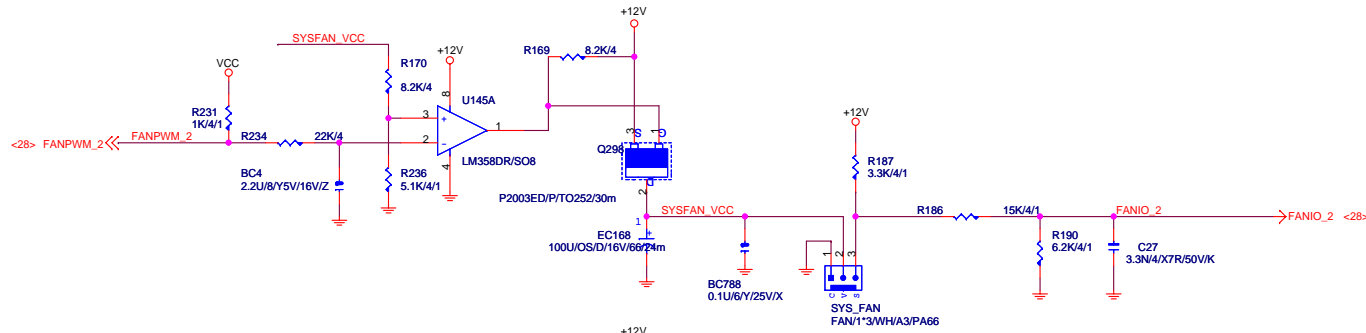




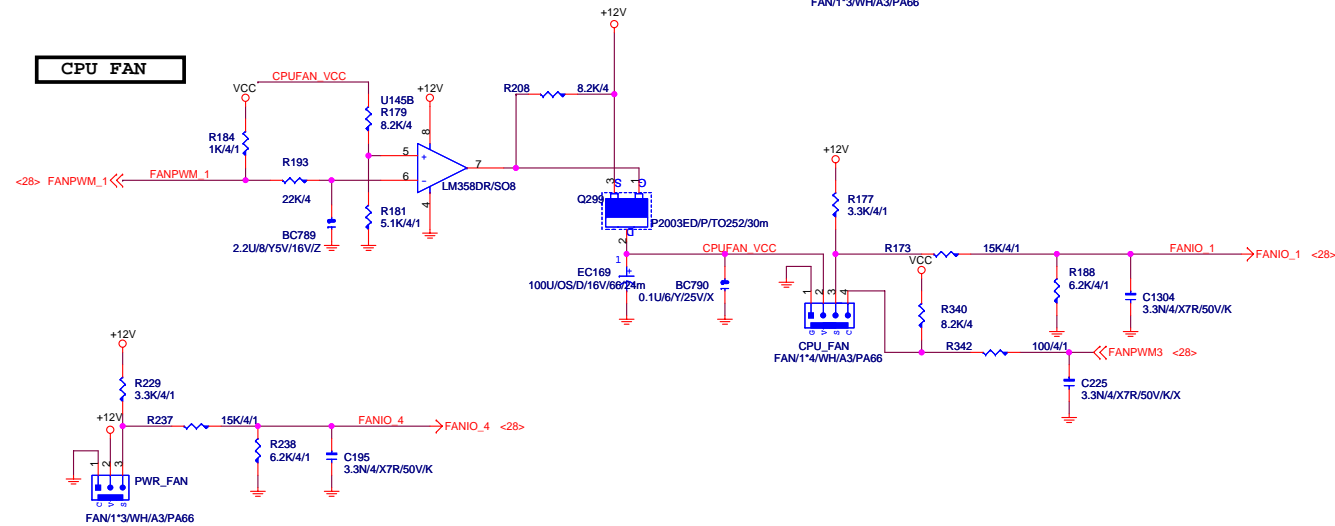
## Hardware Monitor circuits



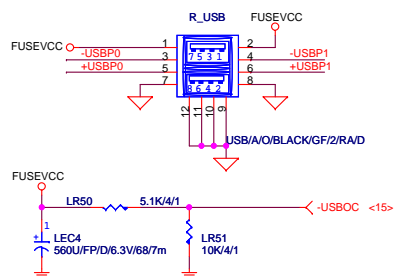
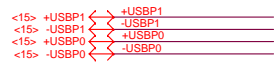
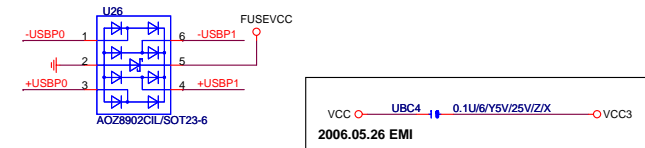
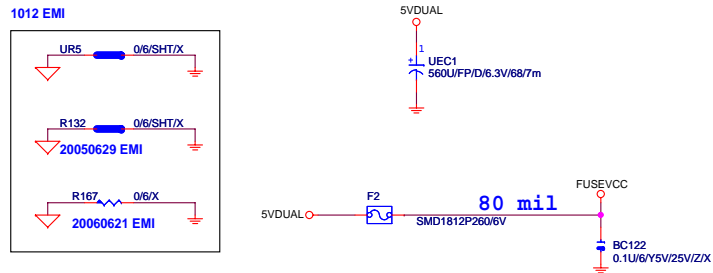
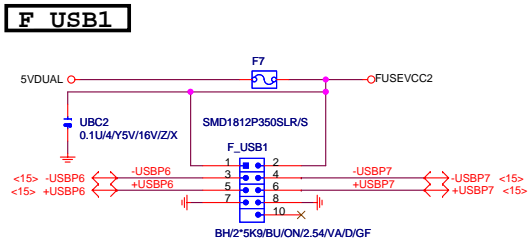
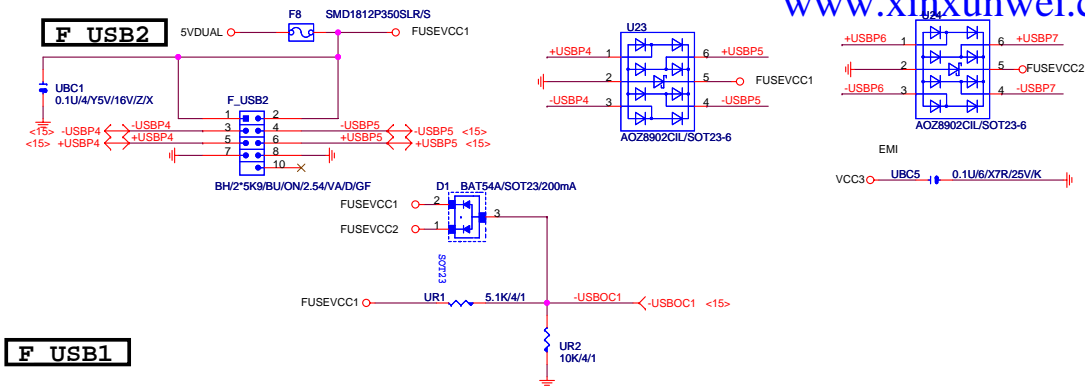
## SYSTEM FAN



## CPU FAN

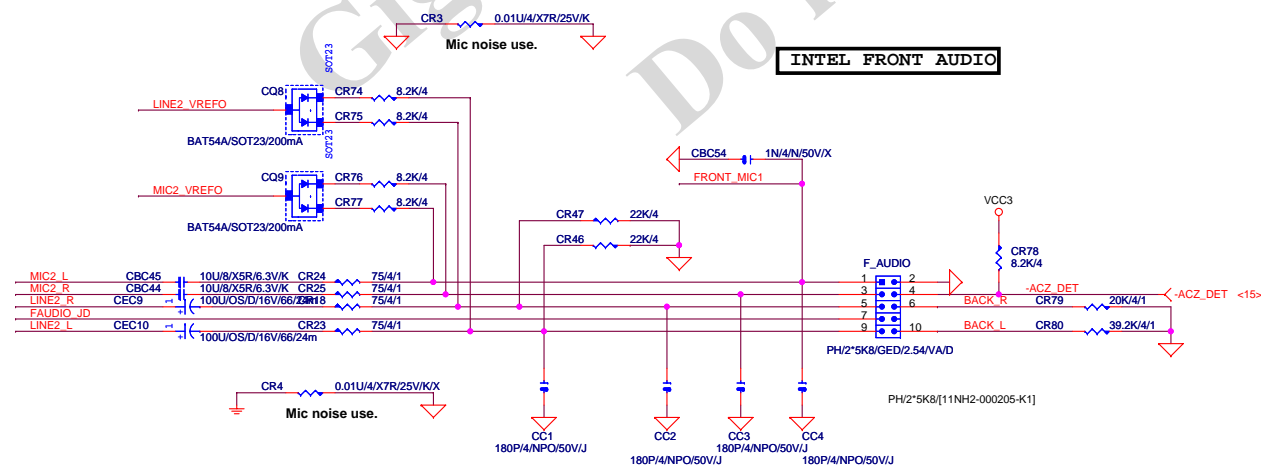
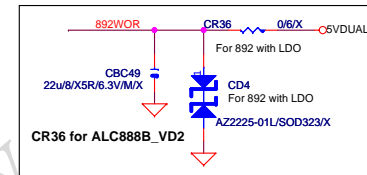
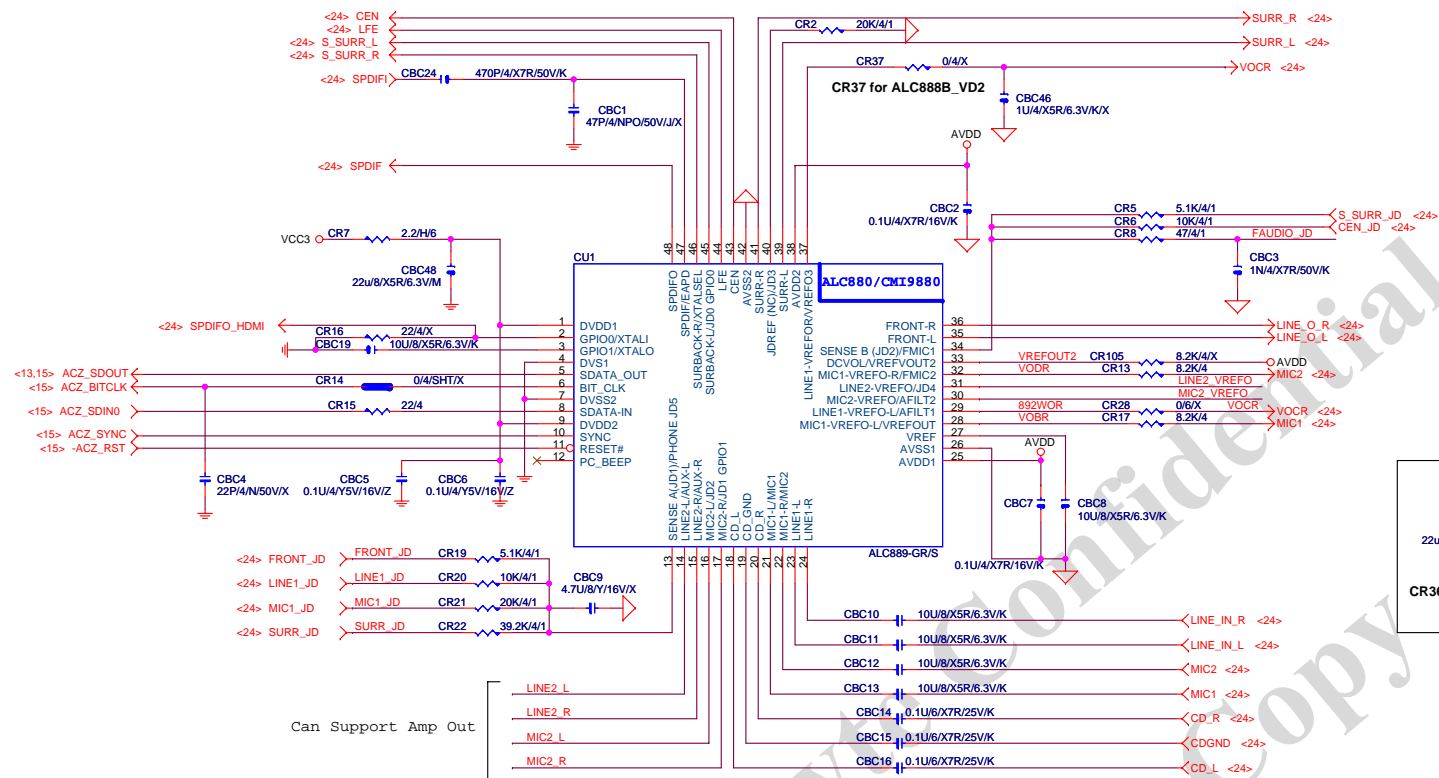






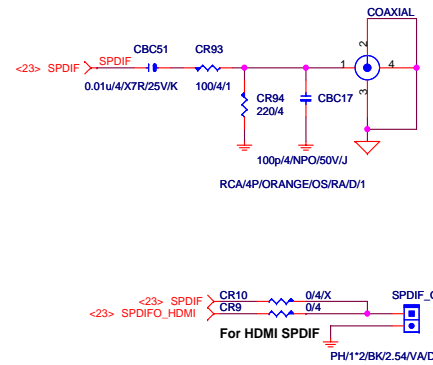
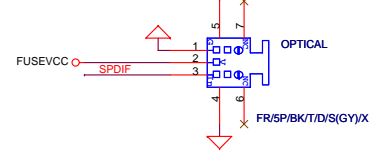
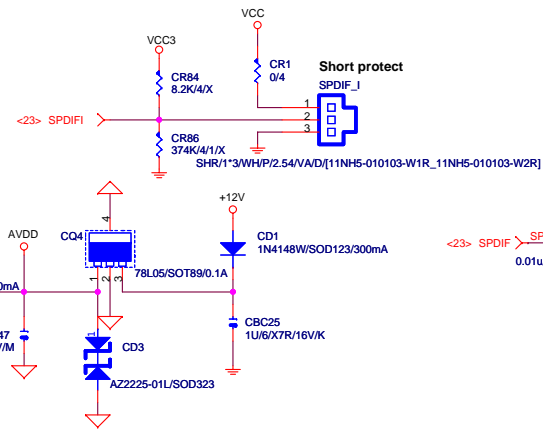
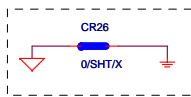
GIGABYTE

Title			
USB PORT			
Size	Document Number	Rev	
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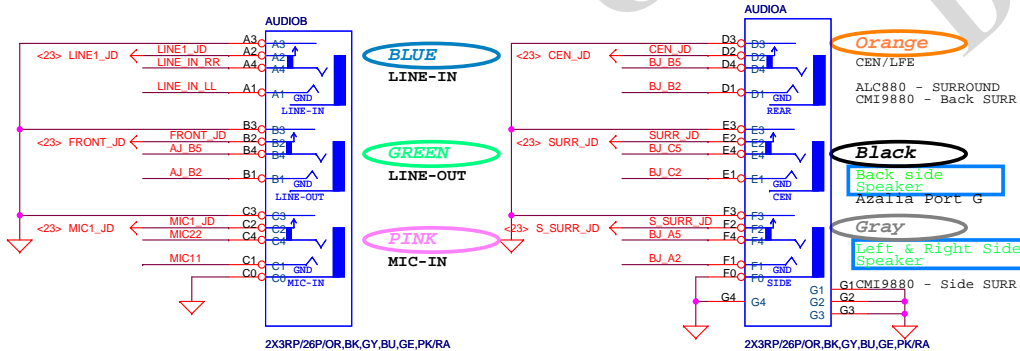
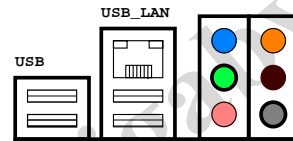
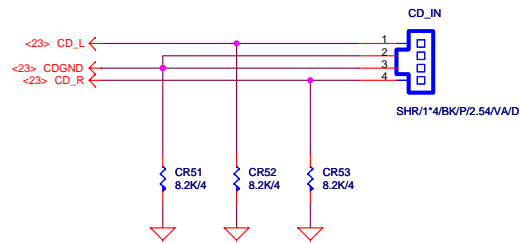


GIGABYTE

Title			AC97 ALC658
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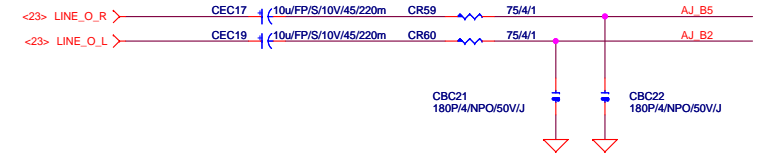


## CD IN

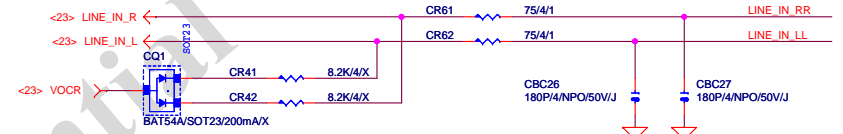


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3RJ+15F/[11NR6-403004-11]

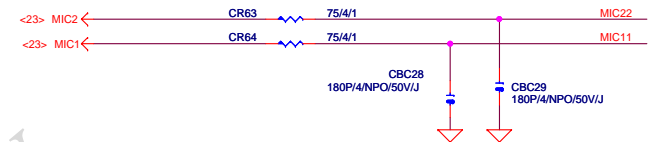
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3RJ+15F/[11NR6-403004-31]

LINE OUT  
FRONT OUT

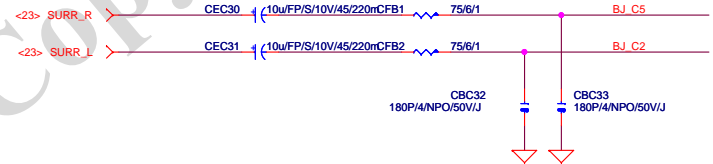
## LINE-IN



## MIC



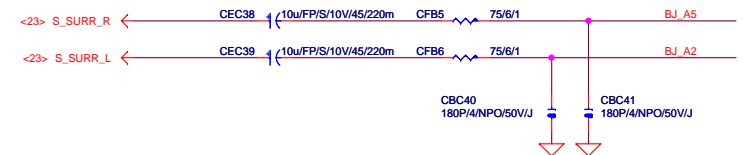
## SURROUND



## CEN/LFE



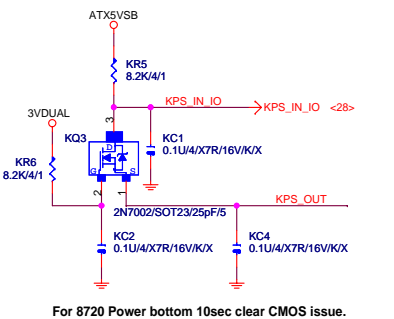
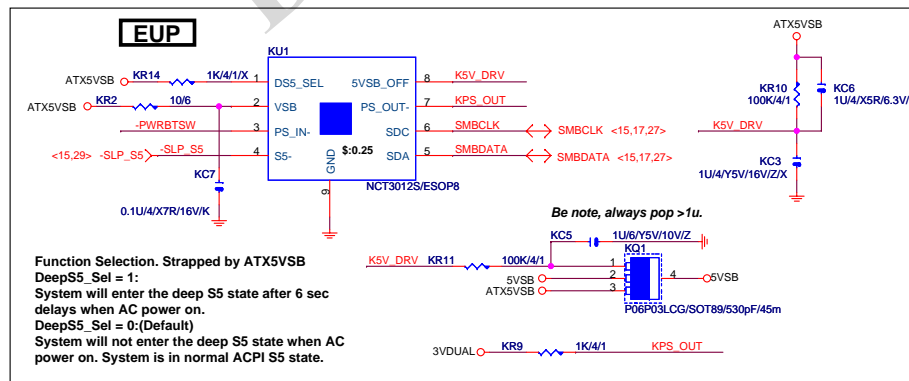
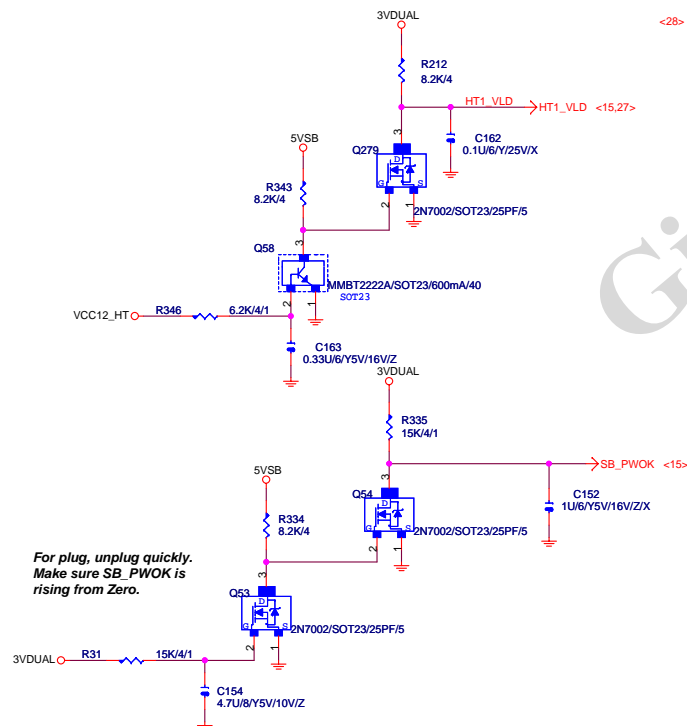
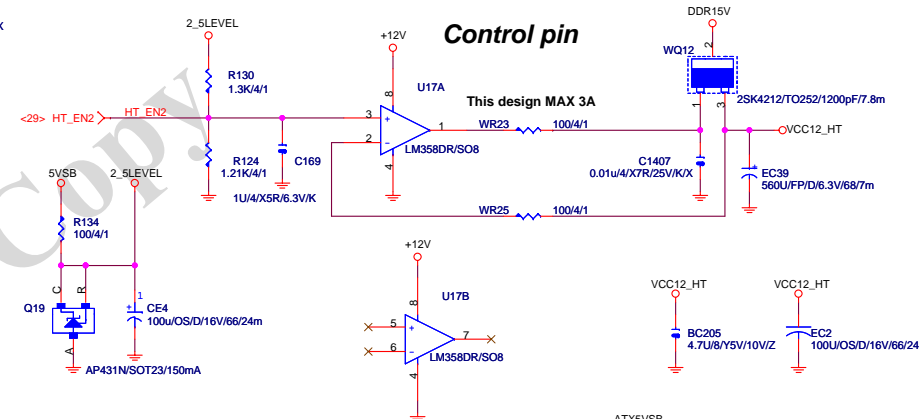
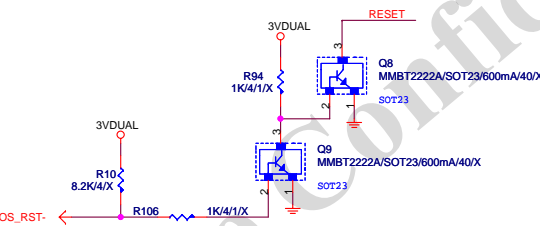
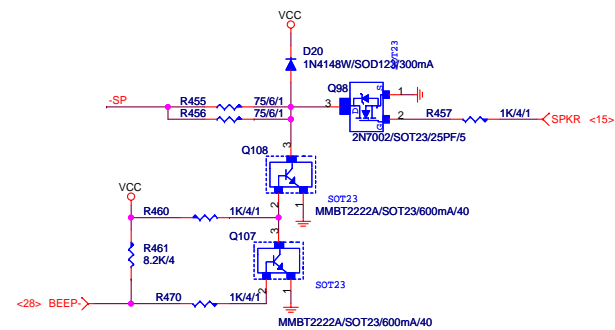
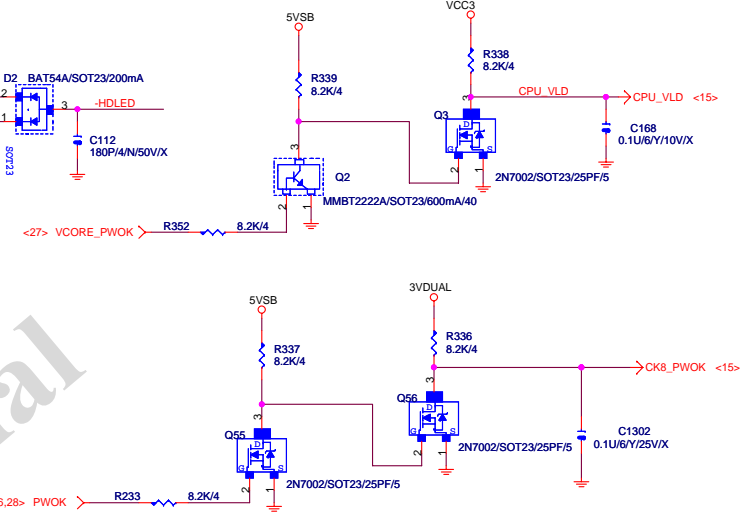
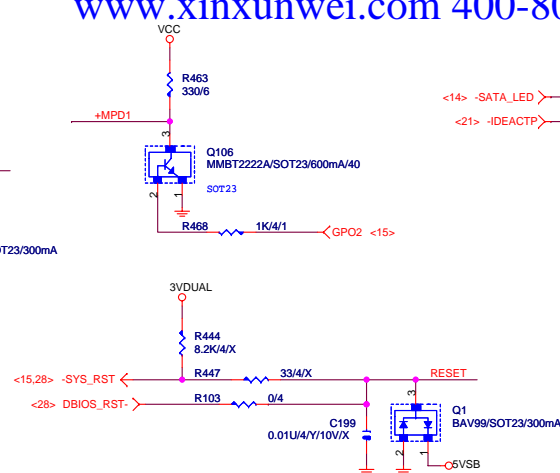
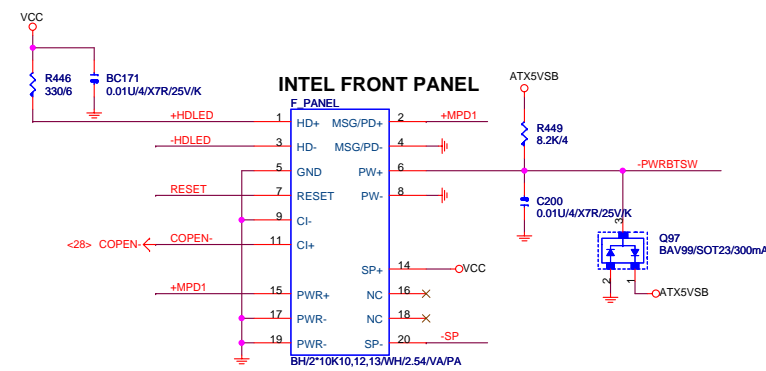
## SURR BACK



GIGABYTE

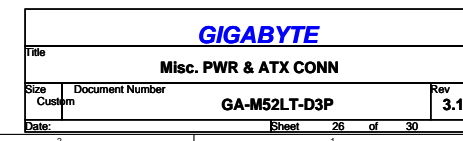
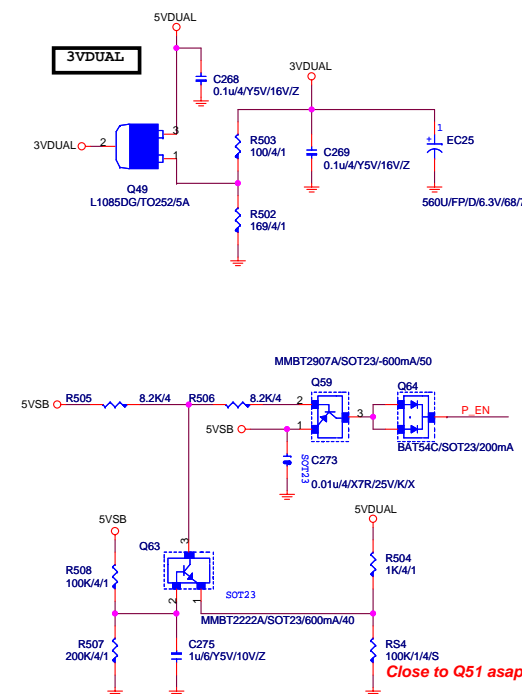
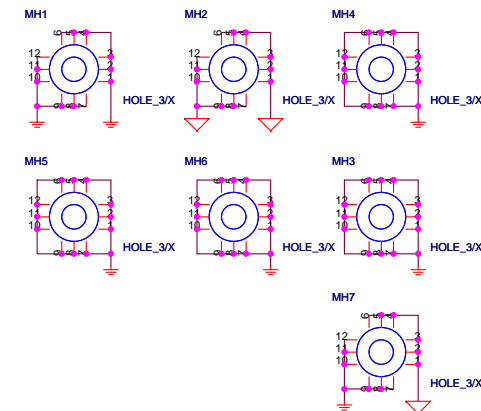
Title		
AUDIO JACK		
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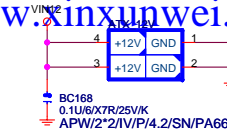




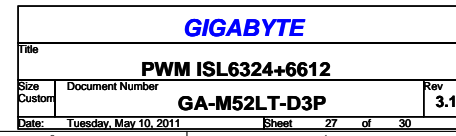
**For plug, unplug quickly.  
Make sure SB\_PWOK is  
rising from Zero.**

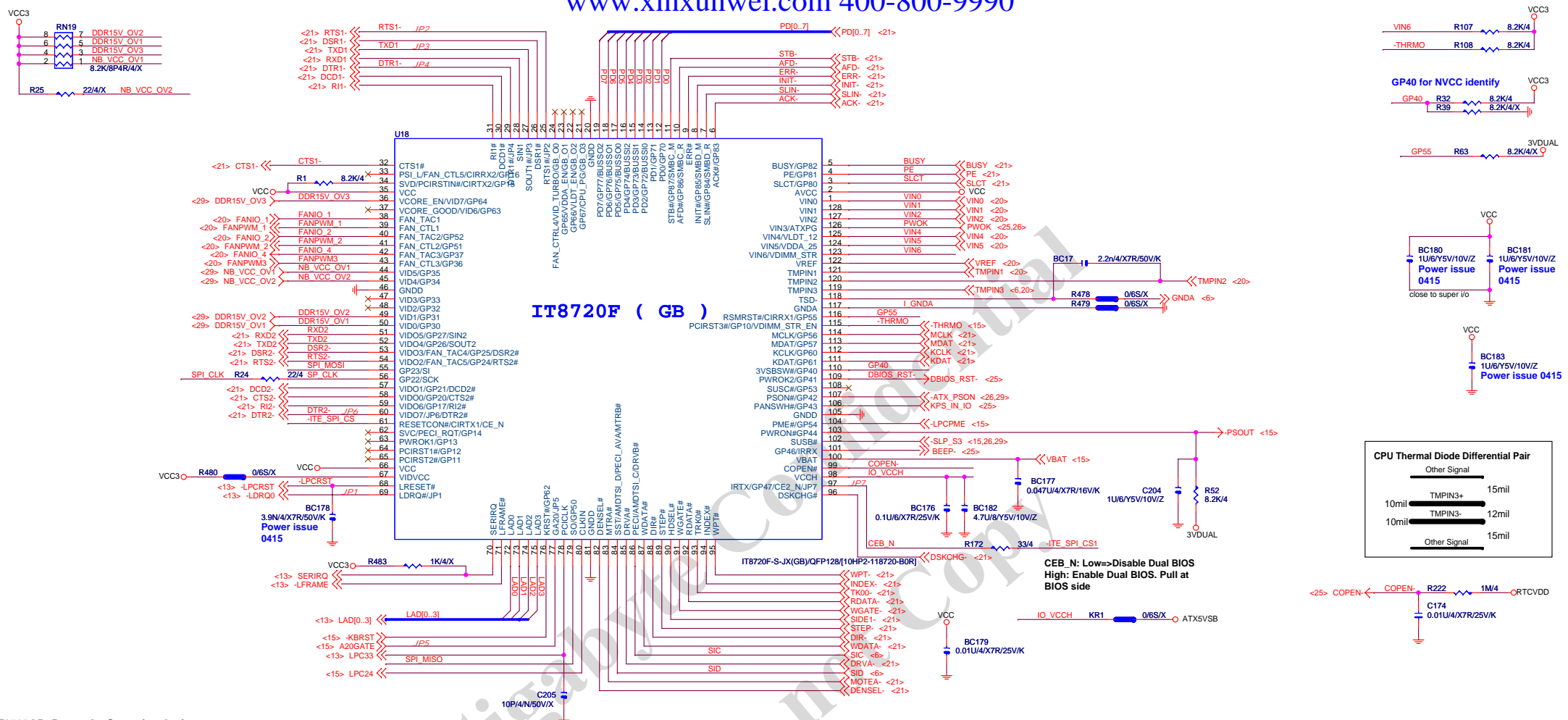
**For 8720 Power bottom 10sec clear CMOS issue.**





**Layout Guide: 1. PWM 2nd layer use GND.  
2. UGATE/PHASE/LGATE:25/25/5~10/25/25.  
3. Isen: 20/5/5/5/20. NB cofeback: 10/10/10**

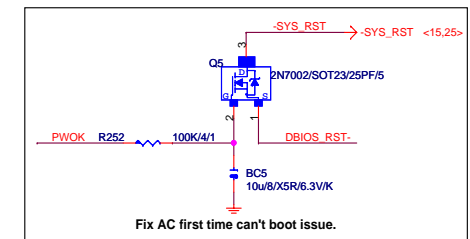
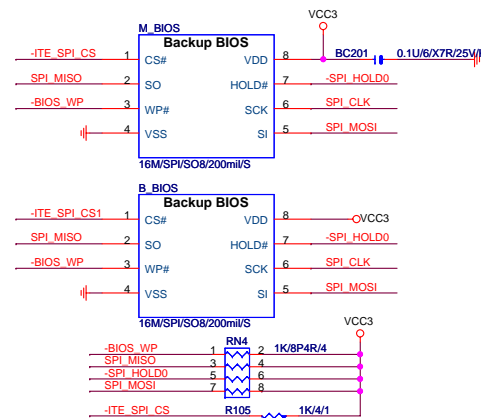
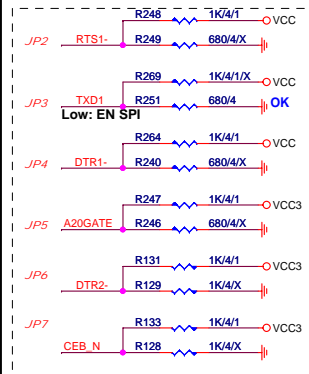


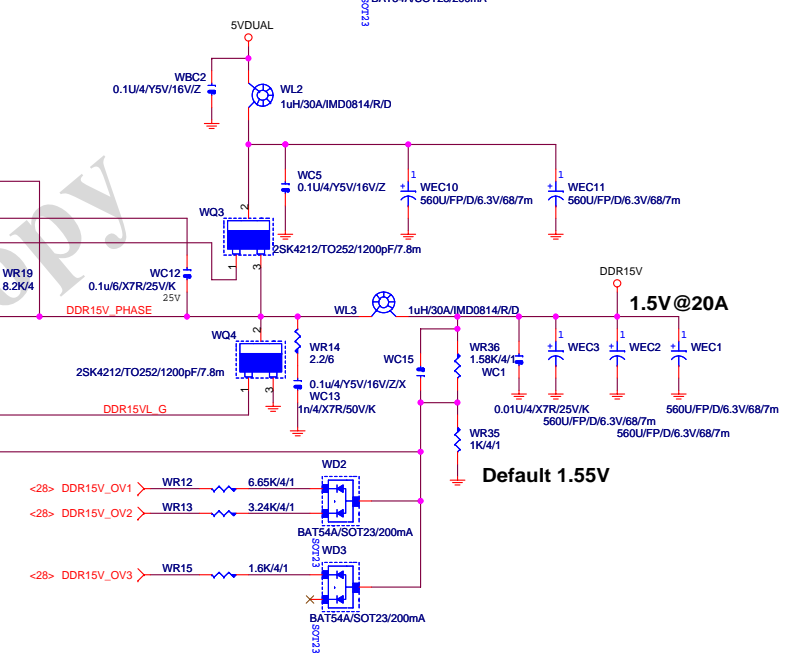
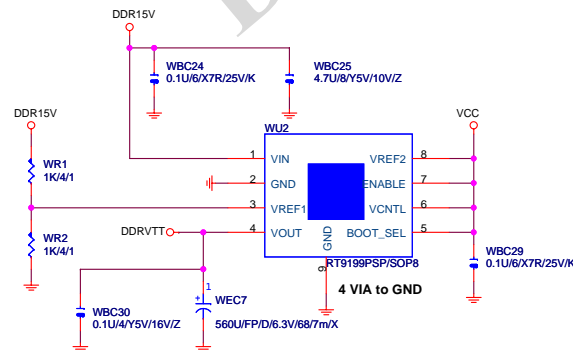
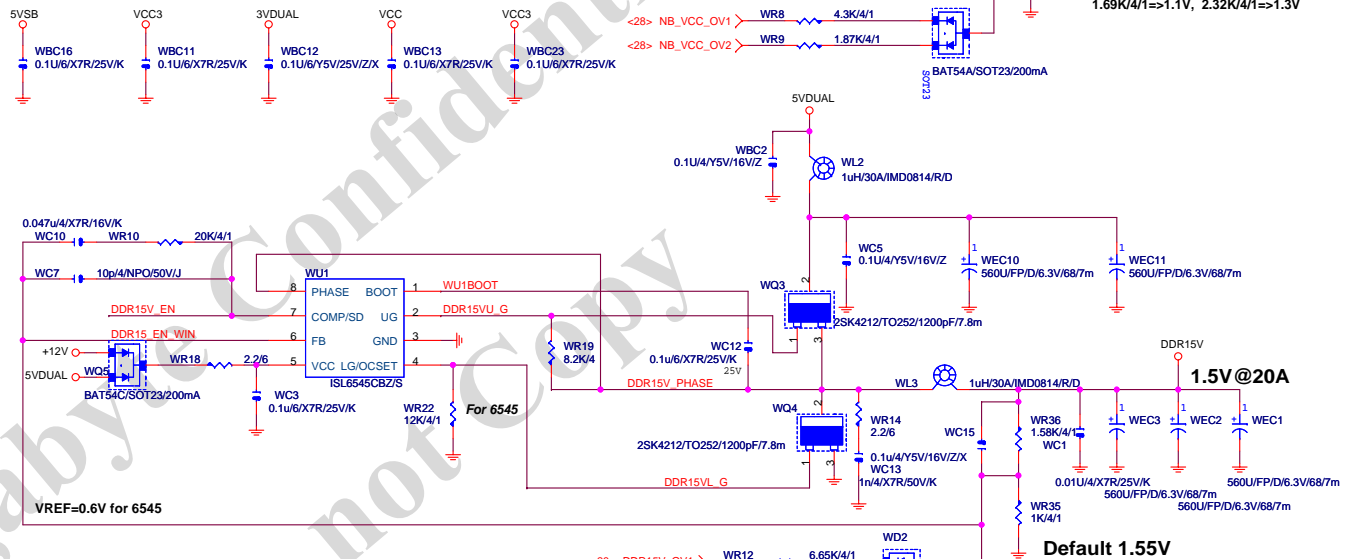
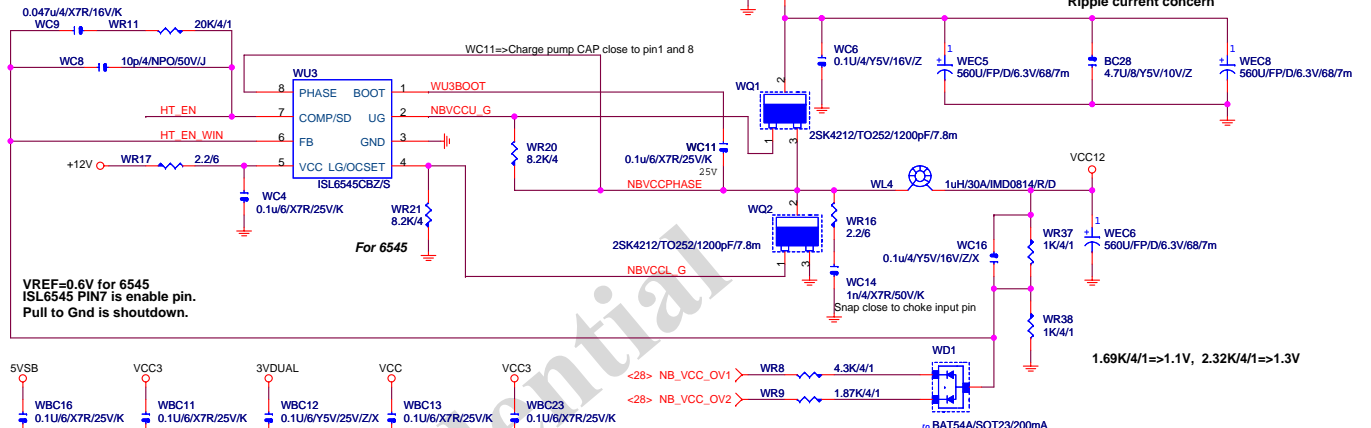
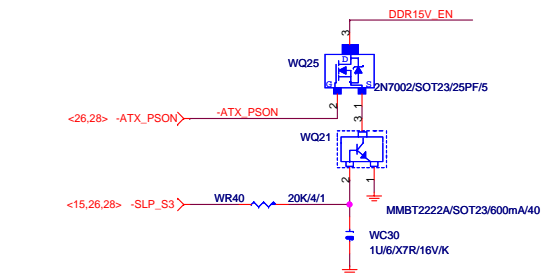
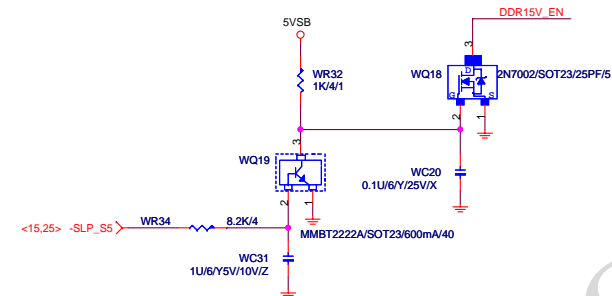
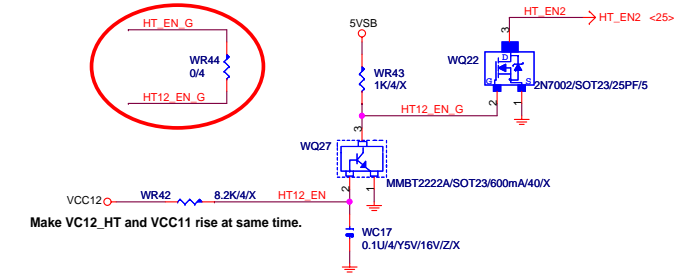
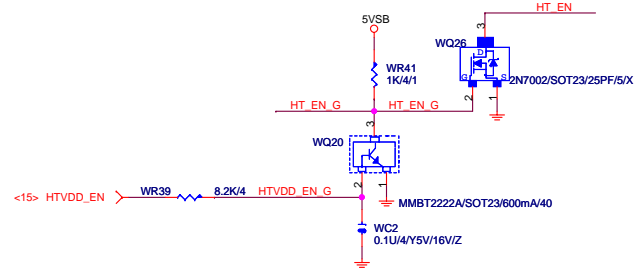


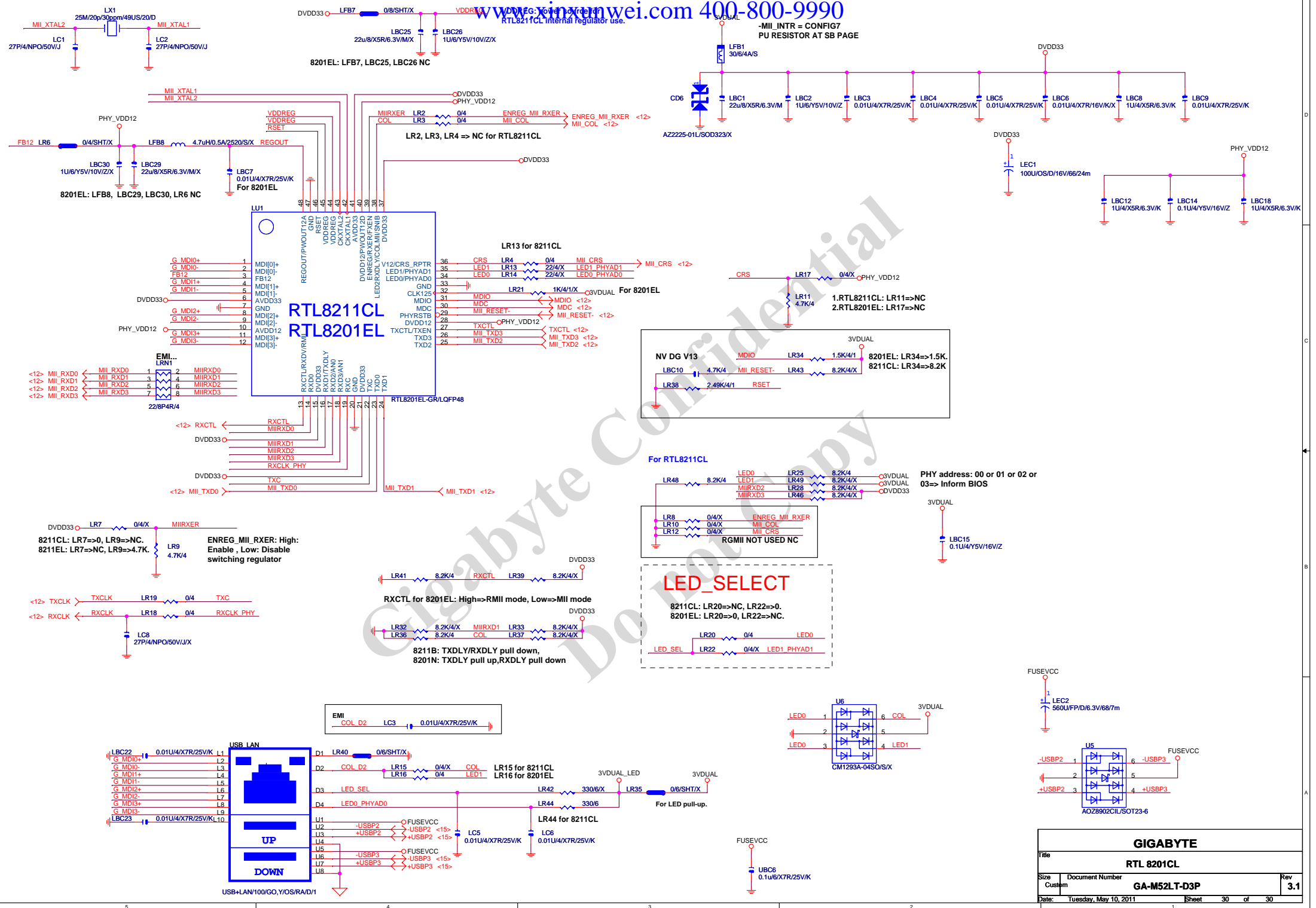
IT8720GB Power On Strapping Options

Symbol	value	Description
JP1	Flashseg1_EN	1 Disabled.
Pin 69	Flash I/F Address Segment 1 is enabled	
JP2	VIDO_EN	1 Disable VID output pins
Pin 25	VIDO_EN	0 Enable VID output pins
JP3	CHIP_SEL	Chip selection in Configuration
Pin 27	CHIP_SEL	
JP4	K8PWR_EN	1 K8 power sequence disabled
Pin 29	K8PWR_EN	0 K8 power sequence enabled
JP3 & JP5	FAN_CTL_SEL	11 Half Run Default value of EC Index 15h/16h/17h is 40h
Pin 27 & Pin 77	FAN_CTL_SEL	10 No Run Default value of EC Index 15h/16h/17h is 7Fh
		01 Full Run Default value of EC Index 15h/16h/17h is 00h
		00 75% Run Default value of EC Index 15h/16h/17h is 20h
JP5	WDT_EN	1 Disable WDT to rest PWROK
Pin 77	WDT_EN	0 Enable WDT to rest PWROK
JP6	SVID_EN	1 Disable SVID Function
Pin 60	SVID_EN	0 Enable SVID Function
JP7	Dual_BIOS_EN	1 Enable Dual BIOS Function for GigaByte Only
Pin 97	Dual_BIOS_EN	0 Disable Dual BIOS Function for GigaByte Only

IT8720CX-&gt;FX(and later) strapping change. JP1 no use, JP3 change to Low.







GIGABYTE			
RTL 8201CL			
Title	Document Number	Rev	
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